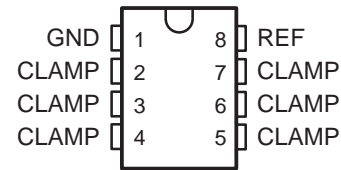


- Protects Against Latch-Up
- 25-mA Current Sink in Active State
- Less Than 1-mW Dissipation in Standby Condition
- Ideal for Applications in Environments Where Large Transient Spikes Occur
- Stable Operation for All Values of Capacitive Load
- No Output Overshoot

D OR P PACKAGE
(TOP VIEW)



description

The TL7726 consists of six identical clamping circuits that monitor an input voltage with respect to a reference value, REF. For an input voltage (V_I) in the range of GND to $< REF$, the clamping circuits present a very high impedance to ground, drawing current of less than 10 μA . The clamping circuits are active for $V_I < GND$ or $V_I > REF$ when they have a very low impedance and can sink up to 25 mA.

These characteristics make the TL7726 ideal as protection devices for CMOS semiconductor devices in environments where there are large positive or negative transients to protect analog-to-digital converters in automotive or industrial systems. The use of clamping circuits provides a safeguard against potential latch-up.

The TL7726C is characterized for operation over the temperature range of 0°C to 70°C. The TL7726I is characterized for operation over the temperature range of -40°C to 85°C. The TL7726Q is characterized for operation over the temperature range of -40°C to 125°C.

AVAILABLE OPTIONS

T_A	SOIC (D)	PLASTIC DIP (P)
0°C to 70°C	TL7726CD	TL7726CP
-40°C to 85°C	TL7726ID	TL7726IP
-40°C to 125°C	TL7726QD	TL7726QP

The D package is available taped and reeled. Add the suffix R to the device type (i.e., TL7726CDR).



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TL7726

HEX CLAMPING CIRCUITS

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Reference voltage, V_{ref}	6 V
Clamping current, I_{IK}	± 50 mA
Junction temperature, T_J	150°C
Package thermal impedance, θ_{JA} (see Notes 1 and 2): D package	97°C/W
P package	127°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
2. The package thermal impedance is calculated in accordance with JEDEC 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Reference voltage, V_{ref}		4.5	5.5	V
Input clamping current, I_{IK}	$V_I \geq V_{ref}$	25		mA
	$V_I \leq GND$	-25		
Operating free-air temperature range, T_A	TL7726C	0	70	°C
	TL7726I	-40	85	
	TL7726Q	-40	125	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK+}	Positive clamp voltage	$I_I = 20$ mA	V_{ref}		$V_{ref} + 200$	mV
V_{IK-}	Negative clamp voltage	$I_I = 20$ mA	-200		0	mV
I_Z	Reference current	$V_{ref} = 5$ V		25	60	μ A
I_I	Input current	$V_{ref} - 50$ mV $\leq V_I \leq V_{ref}$			10	μ A
		$GND \leq V_I \leq 50$ mV		-10		
		50 mV $\leq V_I \leq V_{ref} - 50$ mV		-1	1	

‡ All typical values are at $T_A = 25^\circ\text{C}$.

switching characteristics specified at $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_s	Settling time	$V_{I(system)} = \pm 13$ V, $R_I = 600 \Omega$, $t_t < 1 \mu\text{s}$, Measured at 10% to 90%, See Figure 1		30	μs



PARAMETER MEASUREMENT INFORMATION

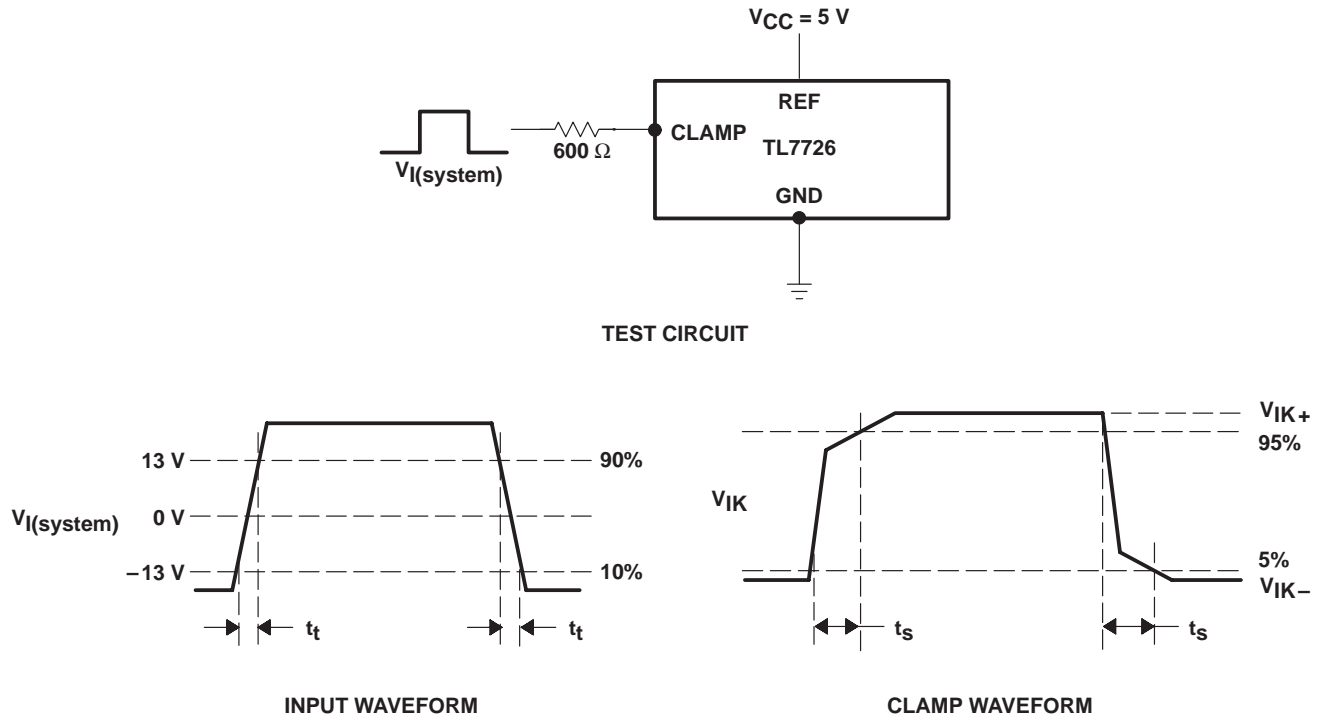


Figure 1. Switching Characteristics

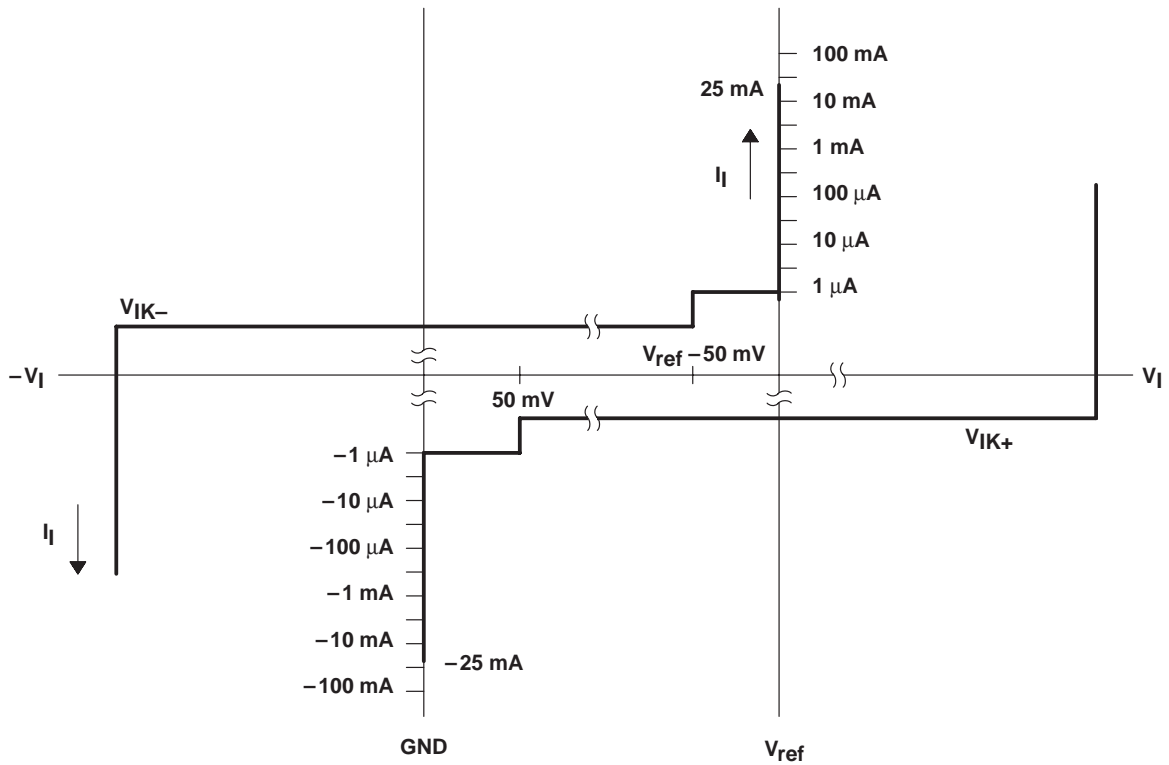
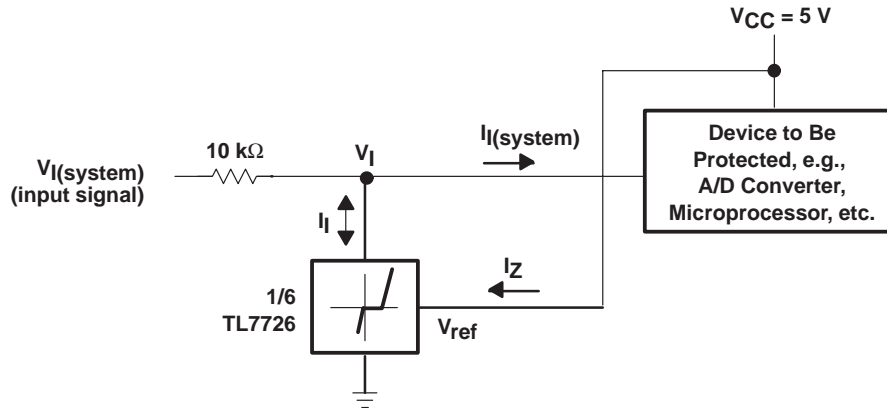


Figure 2. Tolerance Band for Clamping Circuit

TL7726 HEX CLAMPING CIRCUITS

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APPLICATION INFORMATION



Example: If $I_I \gg I(\text{system})$, i.e., $V_I(\text{system}) > V_{ref} + 200\text{ mV}$
where:

$I_I(\text{system})$ = Input current to the device being protected

$V_I(\text{system})$ = Input voltage to the device being protected

then the maximum input voltage

$$\begin{aligned} V_I(\text{system})_{\text{max}} &= V_{ref} + I_{I\text{max}}(10\text{ k}\Omega) \\ &= 5\text{ V} + 25\text{ mA}(10\text{ k}\Omega) \\ &= 5\text{ V} + 250\text{ V} \\ &= 255\text{ V} \end{aligned}$$

Figure 3. Typical Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7726CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7726C	Samples
TL7726CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7726C	Samples
TL7726CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7726C	Samples
TL7726CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7726C	Samples
TL7726CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7726CP	Samples
TL7726CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7726CP	Samples
TL7726ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7726I	Samples
TL7726IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7726I	Samples
TL7726IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7726I	Samples
TL7726IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL7726IP	Samples
TL7726IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL7726IP	Samples
TL7726QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7726Q	Samples
TL7726QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		7726Q	Samples
TL7726QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7726Q	Samples
TL7726QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		7726Q	Samples
TL7726QP	OBsolete	PDIP	P	8		TBD	Call TI	Call TI	-40 to 125	TL7726QP	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7726CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7726IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7726QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7726QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7726CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7726IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7726QDR	SOIC	D	8	2500	367.0	367.0	35.0
TL7726QDRG4	SOIC	D	8	2500	367.0	367.0	35.0

P (R-PDIP-T8)

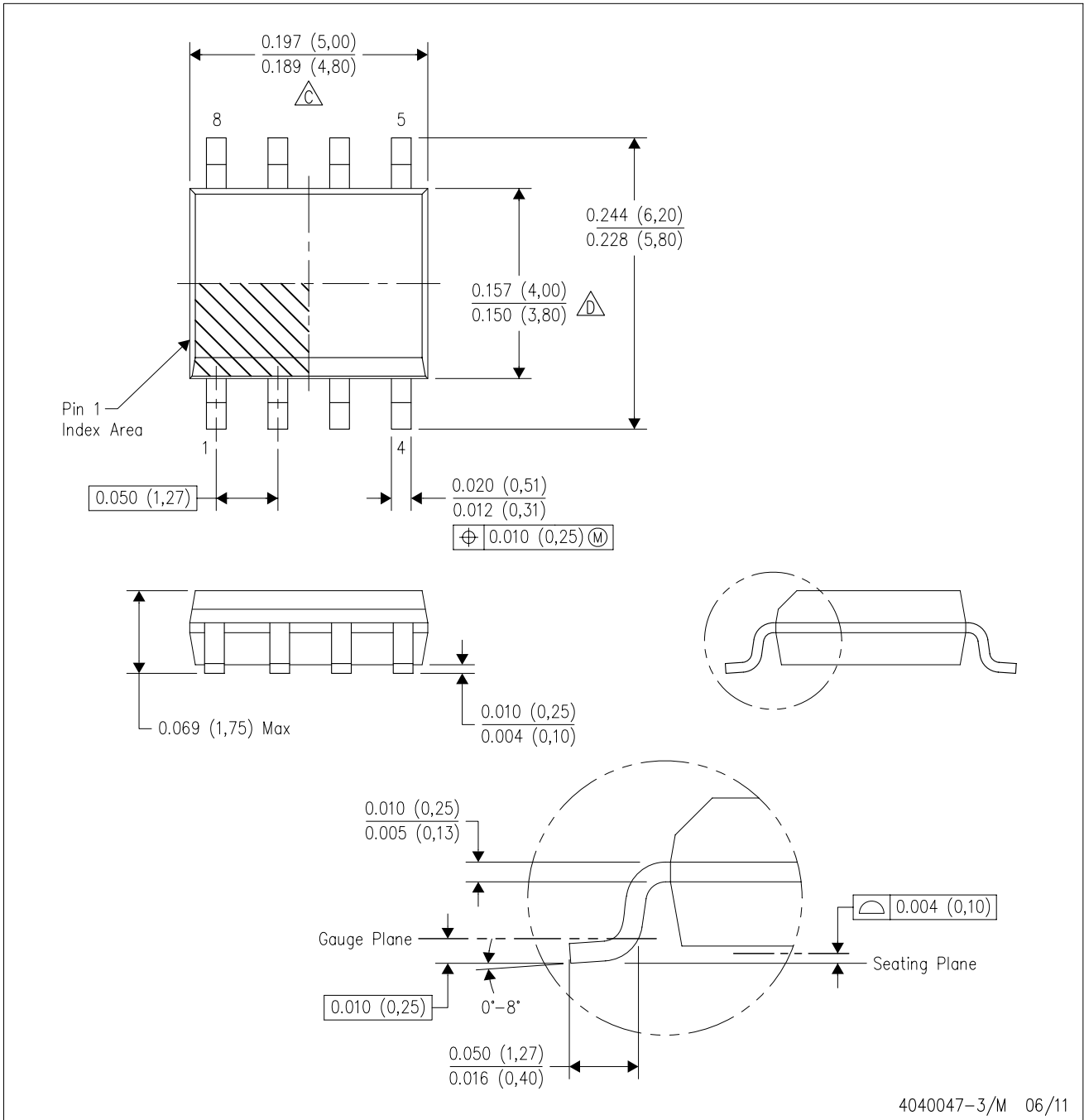
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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